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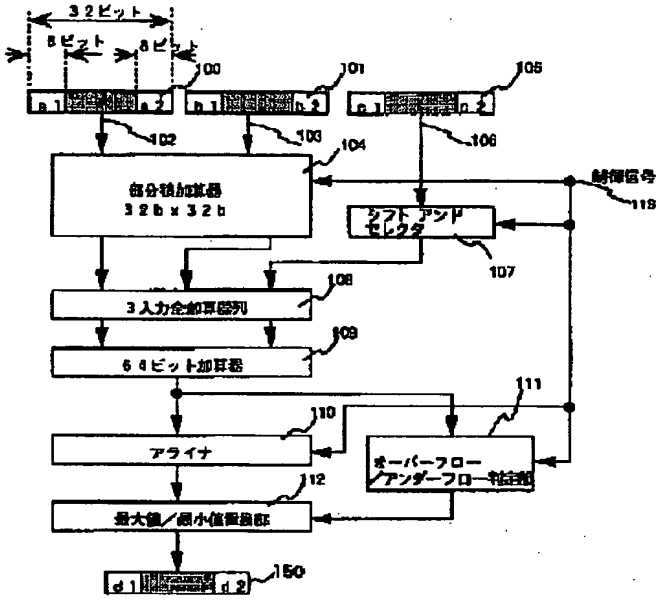
TITLE : COMPUTING ELEMENT AND MICROPROCESSOR



ABSTRACT : PURPOSE: To plural product sum operations at the same times by segmenting data on a total value into values as the multiplication results of respective multiplicands of a 1st register and multipliers of a 2nd register corresponding to them, and finding multiplication results corresponding to pairs of the multiplicands and multipliers as to the respective pairs.

CONSTITUTION: The data on the total sum N+M are used and the two multiplicands a1 and a2 packed in the 1st register 100 and the two multipliers b1 and b2 packed in the 2nd register 101 are inputted to a partial sum adder 104. Then multiplication a1×b1 and multiplication a2×b2 are separately performed. Two addends c1 and c2 packed in a register 105 are inputted and their figures are matched by a shift and selector 107. The two outputs of the partial product adder 104 and the output of the shift and selector 107 are added together and a three-input full-adder array 10864-bit adder 109 can perform product sum operations while a1×b1+c1 and a2×b2+c1 are separated.